ABSTRACT OF THE DISCLOSURE

A matched filter requiring no high-speed processor and which consumes less power is disclosed. Partial filters 301 - 30N obtained by dividing number of matched filter taps by N are provided with a controller 341 for controlling which partial filters are enabled. The controller 341 is supplied with maximum amount of delay of an input signal and with symbol timing. On the basis of the maximum amount of delay, the controller 341 enables only the minimum number of partial filters 301 - 30n that are capable of executing an amount of computation that is required in one symbol period. The enabled partial filters are used multiple number of times per symbol period and the output, each time, integrated sample by sample. Since the disabled partial filters will not operate, it is possible to reduce power consumption and computation time.